Attorney Docket No. 8055-147

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Rolf Weis

SERIAL NO: 10/798,865

FILED: March 12, 2004

FOR: METHOD FOR FORMING A TOP OXIDE WITH NITRIDE LINER

Mail Stop 16
Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR REFUND
(37 C.F.R. §1.28(a)

The amount of $150.00 for extra dependent claims has been charged to the undersigned's Deposit Account. Applicant attaches herewith a copy of the claims of the above-identified application as filed on March 12, 2004, which clearly indicates that the claims do not exceed 20 independent claims. Therefore, Applicant respectfully requests the amount of $150.00 be credited to Deposit Account No. 50-0679.

CERTIFICATION UNDER 37 C.F.R. §1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Director of the U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: March 17, 2005

Frank Chau

II.	FEES CHARGED FOR WHICH REFUND REQUESTED	AMOUNT OF REFUND REQUESTED
__	filing fee	_____
__	surcharge for filing the basic filing fee on a date later than the filing date of the application (37 C.F.R. §1.16(e))	_____
	and/or	
__	surcharge for filing the oath or declaration on a date later than the filing date of the application (37 C.F.R. §1.16(e))	_____
__	extension of term	_____
	__ first month	_____
	__ second month	_____
	__ third month	_____
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X	excess claims	$150.00
__	Issue fee	_____
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__	National Stage fee	_____
	TOTAL REFUND REQUESTED	**$150.00**

NOTE: The refund provisions of §1.28(a) for later submitted small entity statements apply to maintenance fees. Notice of July 30, 1983, 1046 O.G. 28-37.

III. MANNER OF REFUND

Please make refund by

X crediting Deposit Account No. 50-0679

___ refunding payment.

Respectfully requested,

Frank Chau
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What is claimed is:

1. A method for forming a top oxide for a vertical transistor device comprising a poly stud above a polysilicon fill in a deep trench and an isolation region in a portion of the deep trench, comprising the steps of:

forming an etch support nitride liner by low-pressure chemical vapor deposition over the poly stud;

forming a support polysilicon over a portion of the isolation trench outside of an array;

depositing a top oxide over the vertical transistor device;

forming a planarization coating over the top oxide; and

opening the poly stud, wherein the top oxide remains over a portion of the isolation trench.

2. The method of claim 1, further comprising forming a poly cap above the poly-stud above a polysilicon fill in a deep trench.

3. The method of claim 1, wherein forming an etch support nitride liner further comprises forming implants.

4. The method of claim 3, wherein the implants are formed in a well, a support device, or both the well and the support device.

5. The method of claim 1, further comprising performing a support gate oxidation prior to forming the support polysilicon, wherein the poly stud is protected from the support gate oxidation by the etch support nitride liner.

6. The method of claim 1, wherein the step of forming the support polysilicon further comprises:

depositing an etch array polysilicon over the memory device;

applying an etch array mask over a portion of the etch array polysilicon;

etching the etch array polysilicon; and

exposing a pad oxide on the substrate.

7. The method of claim 1, wherein the step of opening the polysilicon stud comprises:

applying a planarization coating; and

etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either high enough to clear the top oxide or, wherein the top oxide in the support can be removed using a mask.

8. The method of claim 1, wherein the step of opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon cap.

9. The method of claim 1, wherein the step of opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating.

10. The method of claim 9, further comprising a timed etch oxide 1:1, removing a portion of the polysilicon cap.

11. A method for forming a top oxide for a vertical transistor device comprising the steps of:

providing a substrate;

forming a storage node in the substrate comprising a deep trench filed with a doped polysilicon;

forming a polysilicon stud above the doped polysilicon in the deep trench;

forming an isolation trench in an upper portion of the storage node and substrate;

forming a patterned etch support liner over a portion of the polysilicon stud, wherein the patterned etch support liner and the doped polysilicon fully encompass the polysilicon stud;

depositing a top oxide over the vertical transistor device;

forming a planarization coating over the top oxide; and

opening the stud to expose the polysilicon stud, wherein portions of the top oxide are preserved above the substrate and above the isolation trench.

12. The method of claim 11, wherein forming the isolation trench further comprises:

forming a pad nitride over a portion of the deep trench memory device exposing a portion of the substrate and the polysilicon stud;

etching an isolation trench in the exposed portion of the substrate and the polysilicon stud;

filling the isolation trench with an insulating material;

removing the pad nitride to expose the substrate; and

performing an oxide deglaze.

13. The method of claim 11, wherein the step of opening the polysilicon stud comprises etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either

high enough to clear the top oxide or, where the top oxide in the support can be removed by a mask.

14. The method of claim 11, wherein the step of opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon cap.

15. The method of claim 11, wherein the step of opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating.

16. The method of claim 15, further comprising a timed etch oxide 1:1, removing a portion of the polysilicon cap.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Weis	Attorney Docket:	8055-147 (02 P 03330 US)
Filed:	March 12, 2004	Examiner:	Unknown
Serial No.:	10/798,865	Art Unit:	2812
Title:	Method for Forming a Top Oxide with Nitride Liner		

Mail Stop: Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination on the merits, Applicant respectfully submits this Preliminary Amendment and remarks as set forth below.

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REMARKS

Claims 1-16 were originally filed in the present application. Claims 1, 3 and 11 have been amended and claims 17-23 are added herein. Accordingly, claims 1-23 are currently pending in the present application.

Applicant respectfully requests that this amendment be entered prior to examination. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at the address below.

Respectfully submitted,

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